

JU-6 SERVICE NOTES

First Edition

SPECIFICATIONS

- Keyboard: 61 Keys (5 octaves) C2-C7

VCF: Cutoff frequency (4Hz-40kHz)

ENV modulation (10 octaves max.)

LFO modulation (6 octaves max.)

Keyboard follow (0-100%)

ENV: Attack time (1ms-3s)

Decay time (2ms-12s)

Sustain level (0-100%)

Release time (2ms-12s)

LFO: Rate (0.3Hz-20Hz)

Delay (0-2.5s)
- Arpeggio: Rate (1.5Hz-50Hz)

Bender control range: DCO (±7 keys max.)

VCF (±4 octaves max.)

Output level: L(−30dBm)/M(−15dBm)/H(0dBm)

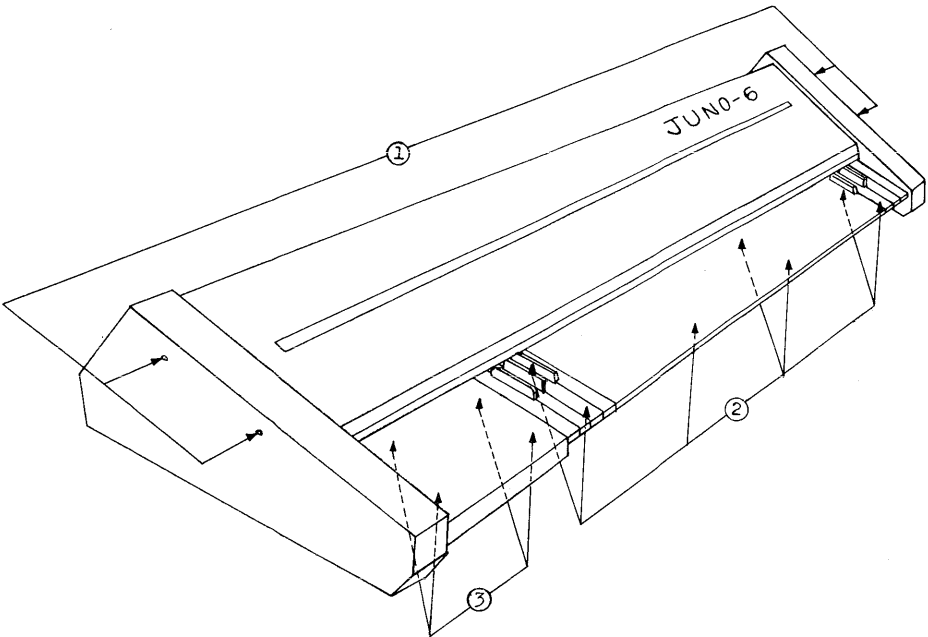
Output: (mono, stereo)

Tune: (±50cents)

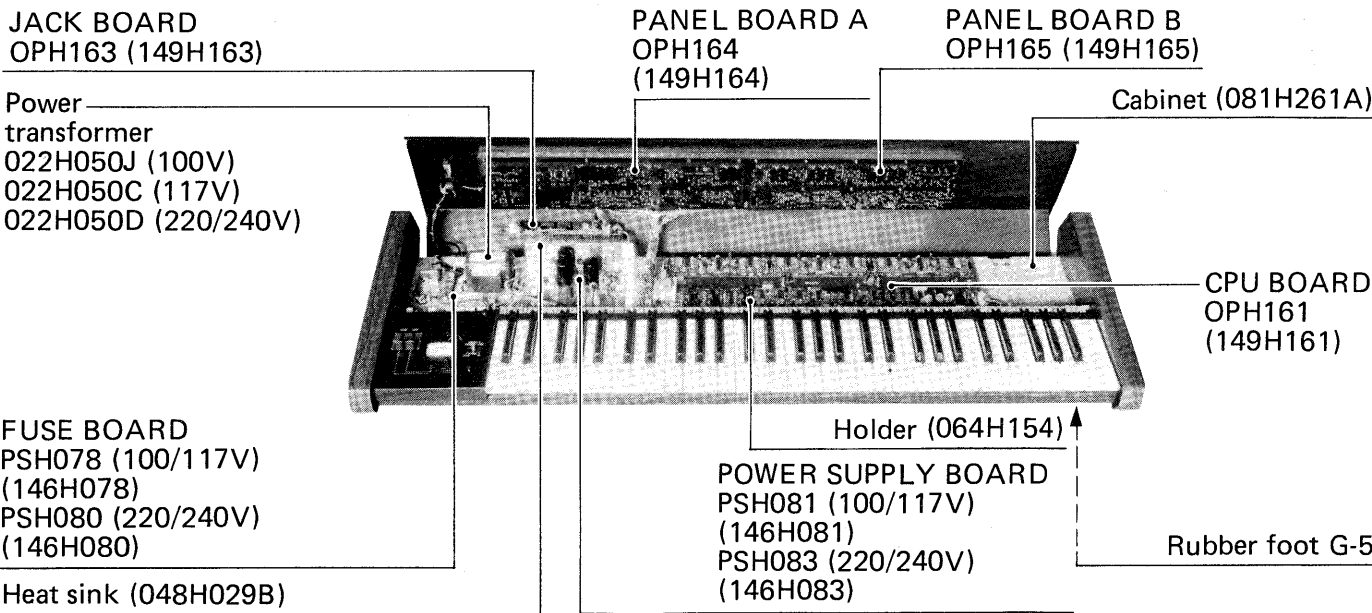
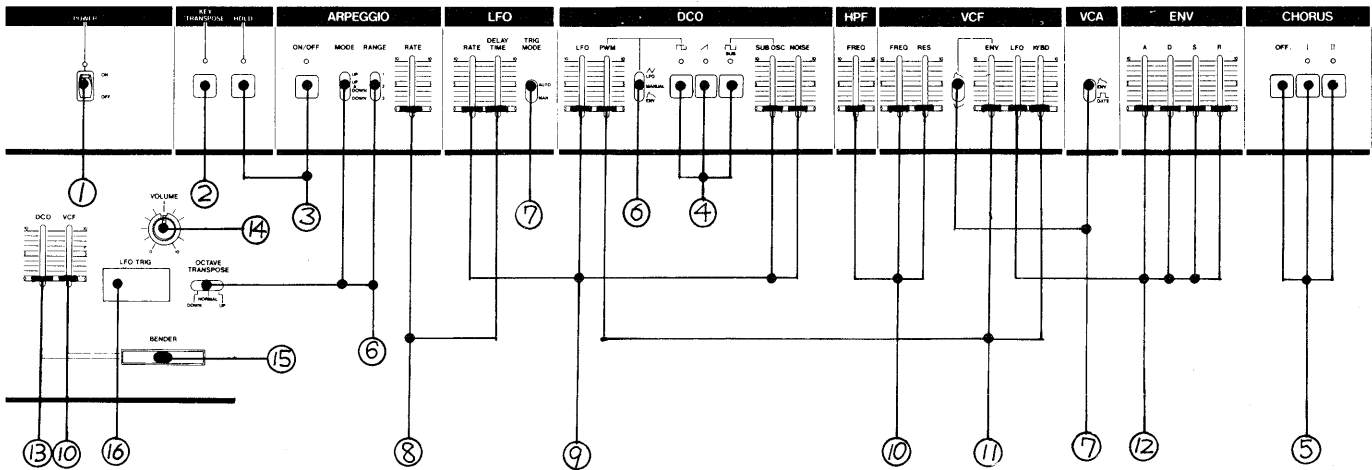
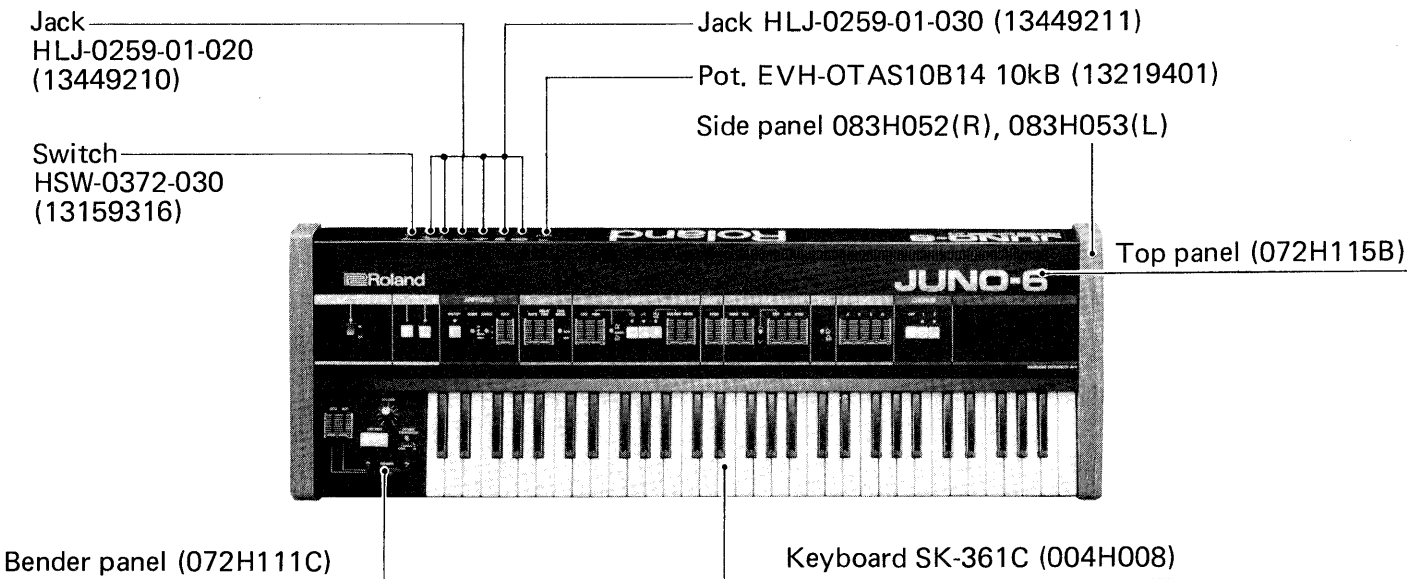
Dimension: 1060(W) x 113(H) x 378(D) mm

Weight: 11kg

Power: 25W



- ①: Top panel removal screws
Joint 3 x 35mm (116H008)
- ②: Keyboard removal screws
4 x 15mm truss Fe Br
- ③: Bender panel removal screws
TP 3 x 15mm pan Fe Br



1	Switch	1801-0121 (13149102)	
2	Switch	SUT11A-1 (13129321)	Button orange (016H029) yellow (016H030) white (016H036)
3	Switch	SUT11A-2 (13129322)	
4	Switch	SUT32A-1 (13129531)	
5	Switch	SUT32A-2 (13129532)	
6	Switch	SLE-623-18P (13139135)	Knob (016H004)
7	Switch	SLE-622-18P (13139136)	
8	Pot.	EVA-TOHC14A16 1MA (13339418)	
9	Pot.	EVA-TOHC14A54 50kA (13339410)	
10	Pot.	EVA-TOHC14B54 50kB (13339419)	
11	Pot.	EVA-TOHC14B14 10kB (13339409)	
12	Pot.	EVA-TOHC14B15 100kB (13339411)	
13	Pot.	EVA-TOHC14A14 10kA (13339416)	
14	Pot.	EWJ-EJAP20B14 10kB x 2 (13219759)	Knob (22470128)
15	Bender assy	PB-4 (029-022)	
16	Switch w/key top	KEH10003 (13129717)	
	All LEDs	TLR124 (15029103)	

PARTS LIST

KEYBOARD
004H008 SK-361C (61 Keys)

CASE
081H261A Cabinet
083H052 Side panel (right)
083H053 Side panel (left)
072H115B Top panel
072H111C Bender panel
064H154 Holder
Rubber foot G-5

KNOB, BUTTON
22470128 Knob
016H004 Knob
016H029 Button (orange)
016H030 Button (yellow)
016H036 Button (white)
12479703 KT3-2 (Key top) (ivory)

POWER SWITCH
1314910 1801-0121

PUSH SWITCH
13129321 SUT11A-1
13129322 SUT11A-2
13129531 SUT32A-1
13129532 SUT32A-2

LEVER SWITCH
13139136 SLE-622-18P
13139135 SLE-623-18P

SLIDE SWITCH
13159316 HSW-0372-01-030

KEY SWITCH UNIT
13129717 KEH 10003 w/key top KT3-2
13129714 KEH 10903 switch proper
13129719 Guide pin CHC32801A
22269208 Cushion rubber CK42602A

PCB
149H161B CPU board OPH161B
(etch mask 052H370B)
149H164A PANEL board A OPH164A
(etch mask 052H372A)
149H165A PANEL board B OPH165A
(etch mask 052H373A)
149H162A BENDER board OPH162A
(etch mask 052H371A)
149H163A JACK board OPH163A
(etch mask 052H374A)
146H081A POWER SUPPLYboard PSH081A (100/117V)
146H083A POWER SUPPLY board PSH083A (220/240V)
(etch mask 052H369A)
146H078A FUSE board PSH078A (100/117V)
146H080A FUSE board PSH080A (220/240V)
(etch mask 052H348A)

JACK
13449211 HLJ-0259-01-030 (mono)
13449210 HLJ-0259-01-020 (stereo)
FUSE
12559331 GGS-0.8A prim. (100V/117V)
12559511 CEE T500mA prim. (220/240V)
12559513 CEE T1.0A sec. (220/240V)

BENDER UNIT
029-022 PB-4

POSISTOR
15229909 ERS-B33G561 560Ω
15229910 ERS-B33G122 1.2KΩ

RESISTOR ARRAY
13829821 RGDS8 x 103K 10K x 8
13910113 RGDS4 x 103K 10K x 4
13910114 RGDS4 x 223K 22K x 4

POTENTIOMETER
Slider
13339416 EVA-TOHC14A14 10kA
13339409 EVA-TOHC14B14 10kB
13339410 EVA-TOHC14A54 50kA
13339419 EVA-TOHC14B54 50kB
13339411 EVA-TOHC14B15 100kB
13339418 EVA-TOHC14A16 1MA

Rotary
13219759 EWJ-EJAP20B14 10kB x 2
13219401 EVH-OTAS10B14 10kB

Trimmer
13299134 RVF8P01-502 5kB
13299135 RVF8P01-103 10kB
13299136 RVF8P01-503 50kB
13299137 RVF8P01-104 100kB
13299553 RVS0707V101-102M 1kB
13299554 RVS0707V101-502M 5kB

COIL
022A018 S167999 37μH

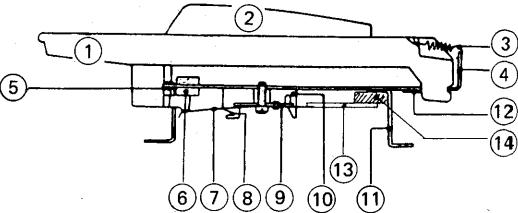
TRANSISTOR
15199113 2SA1015-GR
15119805 2SB834-O
15129114 2SC1815-GR
15129108OA 2SC945 (NZ-noise generator)
15129130 2SC1583-F
15129136 2SC2878-A or B
15129117 2SC1923
15129128 2SC752-Y

DIODE
15019103 1S2473
15029103 TLR124 (LED)
15019249 KV1226X (Varicap)
15019245 1B4B41
15019243 1B4B1

POWER TRANSFORMER
022H050J (100V)
022H050C (117V)
022H050D (220/240V)

IC
15179135 μPD8049C-238 CPU
15159113HO HD14051BP Single 8 CH Multiplexer
15159104HO HD4011BP Quadruple 2-Input NAND Gate
15159105HO HD14013BP Dual D-type Flip-Flop
15159112 TC4049BP Hex Inverter/Buffer
15159116TO TC4069UBP Hex Inverter
15159120TO TC4099BP
15179110MO μPD8253C Triple Programmable Interval Timers
15229801 IR3109 VCF
15229807 IR3R01 ADSR
15229802 BA662 A or B VCA
15169117HO HD7407 Hex Buffers/Drivers
15169310HO HD74LS42 BCO-TO-Decimal Decoder
15189118HO TL082 OP Amp
15189142 TA75558S OP Amp
15189143 TA75559S OP Amp
15189105 μPC4558C OP Amp
15189136BO M5218L OP Amp
020-215 MN3009 BBD
020-224 MN3101 BBD Driver
15199106TO μPC7805 5V Voltage Regulator
15199110TO TA7179P ±15V Voltage Regulator

OTHERS
048H029B Heat sink
12389804 Ceramic resonator CSA11MHz with paired CSC300K
12199515 Fuse holder TF-758

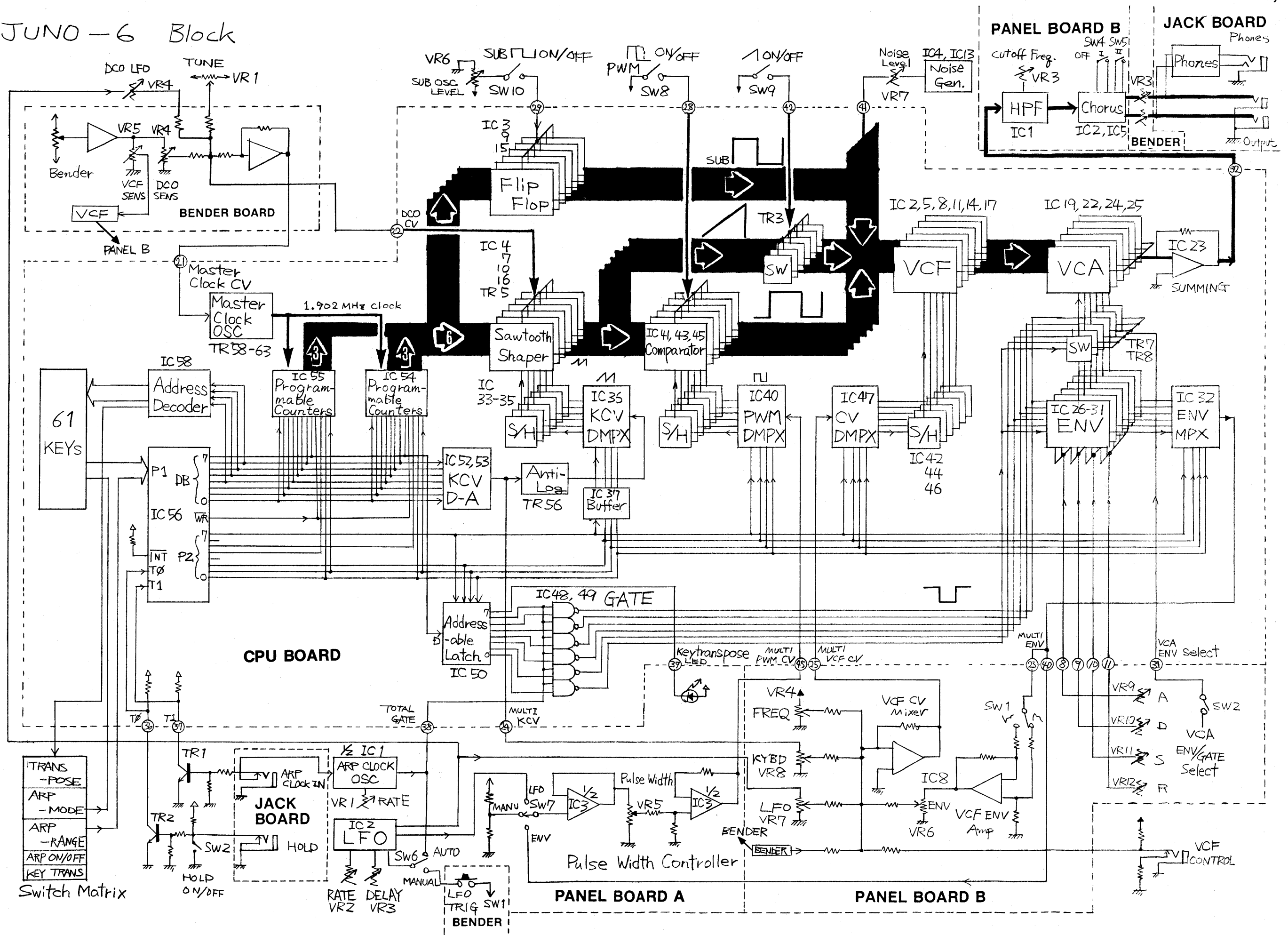


KEYBOARD PARTS
SK-361C (004H008)

NO	PART NO	DESCRIPTION
1	106H026	Natural key C F
1	106H027	Natural key D
1	106H028	Natural key E B
1	106H029	Natural key G
1	106H030	Natural key A
1	106H031	Natural key C' F'
2	106H032	Sharp key black
3	070H029	Key spring H29
4	061H086A	Chassis H86A
5	068H004	Guide bushing H4
6	101H141	Level felt H141
7	071H044	Contact leaf H44
8	071H051	Busbar 8P H51
	071H054	Busbar 5P H54
9	043H007	Switch unit 12P H7
	043H008	Switch unit 13P H8
10	104H029	Busbar holder H29
11	062H024	Chassis bracket H24
12	098H006	Key stopper H6
13	052H283-5	Matrix board H283-5
14	107H059	Cushion H59

NOTE:
Although Roland has employed 8-10 digit coding, old ones (6 digit and 6 digit with H) are still applied to some parts.

JUNO-6 Block



CIRCUIT DESCRIPTION

The JUNO-6 has two circuits not found on the conventional polyphonic synthesizer. They are:

- * Digital controlled oscillator
- * Multiplexed controlling for VCF and PWM

SOUND SOURCE

MASTER OSCILLATOR

An LC oscillator having variable capacitance diode (D18) to which control voltages from BENDER, LFO and TUNE circuitry, common to all the notes, are supplied.

Variable range:
Bender — ±700 cents LFO — ±300 cents TUNE — ±50 cents

When these voltages are summed together, the maximum shiftable range of the master oscillator is ±1050 cents or from 1MHz to 3.5MHz with the center frequency at approximately 1.9MHz. The output signal is routed to programmable counters IC54 and IC55 through TR63.

PROGRAMMABLE COUNTERS IC54 and IC55

Programmable Counter 8253 consists of three 16-bit counters capable of dividing input signal by up to 65535. When master oscillator output is 1902810Hz and divisor is 4305, the counter develops 442Hz rectangular signals.

Each time key(s) is played, division data to the counters is read from CPU's internal PROM and placed at the CPU data bus in 8 bit x 2 format, then sent to DATA IN of the counters.

KEYBOARD AND SWITCH SCANNING

The CPU applies scanning data (in the left column of the table below) to Address Decoder IC58, setting its appropriate output pin low. The pin is connected to 8 key (function) switches tied together in group. The other poles of these switches are connected to the respective input pins of Inverters IC53 and IC57. Contact in this group, has been closed, removes positive voltage at the input pin of the Inverter, which in turn applies high output to Port 1 of the CPU.

CPU 8049-238 stores two kinds of program for use in different applications, one of which must be selected before starting scanning.

After power on reset, CPU first issues bits 1001 (see bottom of the table) and knows that voices to be assigned to keys played are 6 (L, H, L at P10-P12 of PORT 1) and that the model it is now installed is the JUNO-6 (L at P17 of PORT 1). If the CPU malfunctions, voltages on these pins and associated circuits (including D20) should be checked.

KEY ASSIGNMENT

Six channels are assigned to the keys played in the order CH1-CH6, in the cyclic manner, that is, if the 7th key is played while previously played 6 keys are still held, the 7th key steals the first voice.

Three more assignment modes are provided for test purpose. See Adjustment section of this manual.

BUS 6543	PORT-1							
	0	1	2	3	4	5	6	7
0000	C	C#	D	D#	E	F	F#	G
0001	G#	A	A#	B	C	C#	D	D#
0010	E	F	F#	G	G#	A	A#	B
0011	C*	C#	D	D#	E	F	F#	G
0100	G#	A(442)	A#	B	C	C#	D	D#
0101	E	F	F#	G	G#	A	A#	B
0110	C	C#	D	D#	E	F	F#	G
0111	G#	A	A#	B	C	(C#)	(D)	(D#)
1000	TRANPOSE		ARP & KEY ASSIGN		ARP RANGE		ARP ON	KEYTRANS
1001	L	H	L	not in use				L

Table 1

WAVEFORM CONVERSION

When a key is held down, programmable counters IC54 and IC55 create a series of square waves at output pins for assigned channels. Positive and negative going edges of the square wave are converted into pulses in opposite direction by C6 x R34 time constant and applied to the base of TR5 which discharges C7 on negative going pulse. When TR5 shuts off, C7 charges current flowing from S/H IC35. The charging rate should vary with the discharging rate to maintain the sawtooth amplitude constant. The figure below shows how this is accomplished.

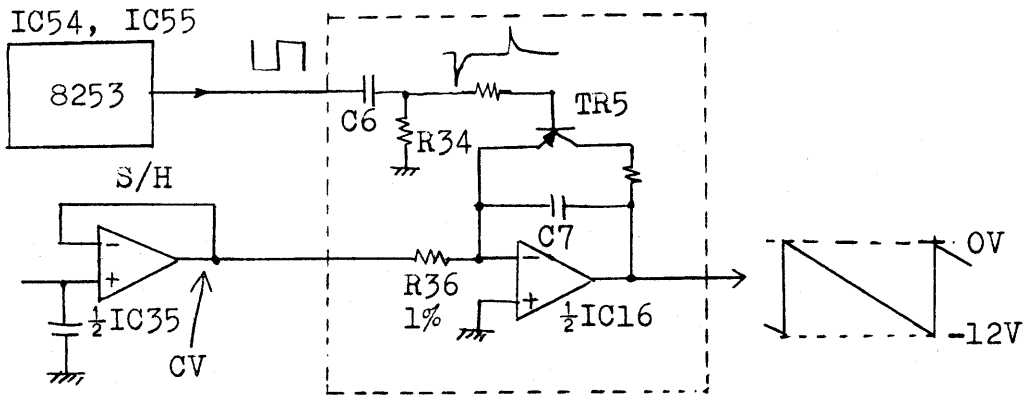


Fig. 1

Analog voltages (a set of 6 key control voltages for 6 channels) from D/A converter change in 0.48V/oct steps as different keys are played. KCVs are combined with voltages from TUNE, LFO and BENDER, if any, and fed to anti-log amplifier TR56. The combined voltage increases or decreases in 1V/oct steps at TR56 output.

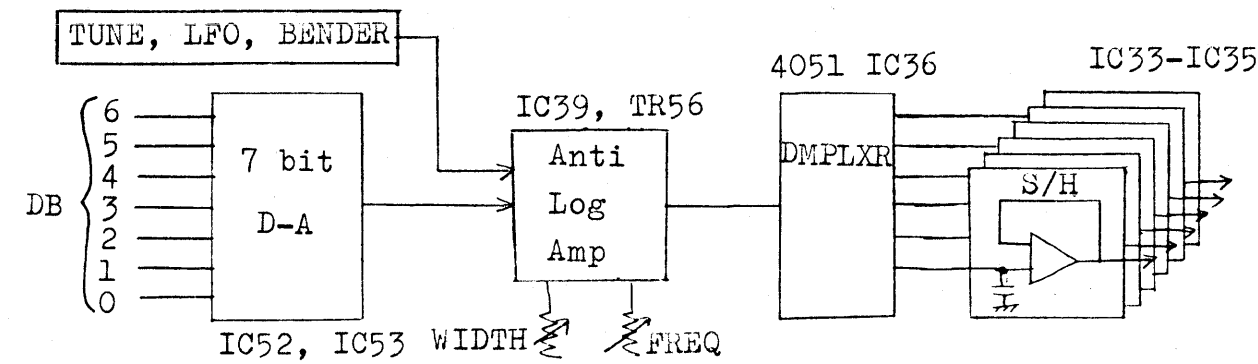


Fig. 2

VARIABLE PULSE WIDTH

Besides its direct application as sound source, sawtooth generator also serves as a source for asymmetrical square wave. Sawtooth wave is routed to (-) pin of comparator/S&H circuit where the voltage on (+) pin determines the sampling period of the sawtooth wave thus duty cycle of the square wave.

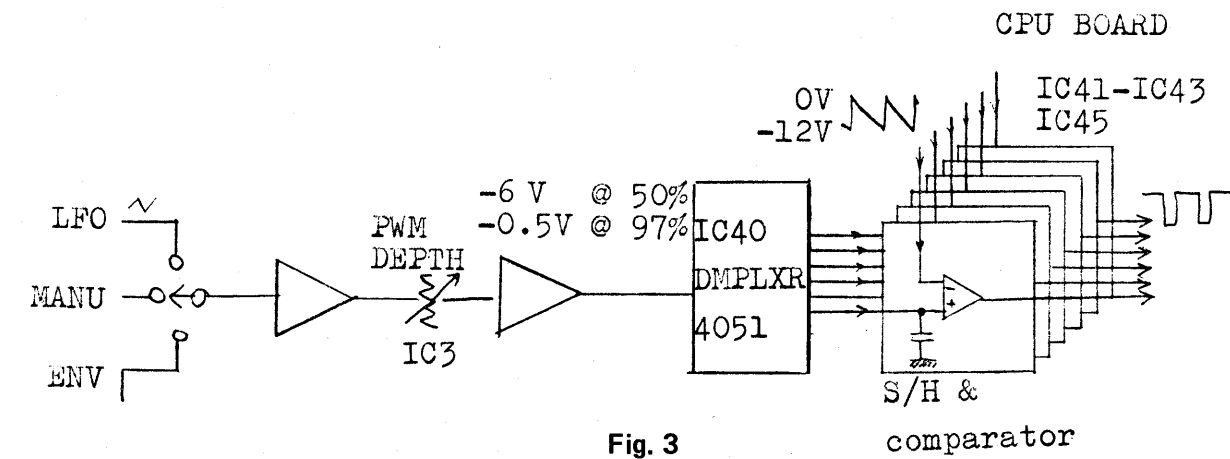


Fig. 3

SUB OSCILLATOR

Square wave from programmable counter is also delivered to flip-flop where it is divided in half, and applied to TR4 base. The amplitude of TR4 output can continuously be varied by setting of SUB VR6 on Panel board A.

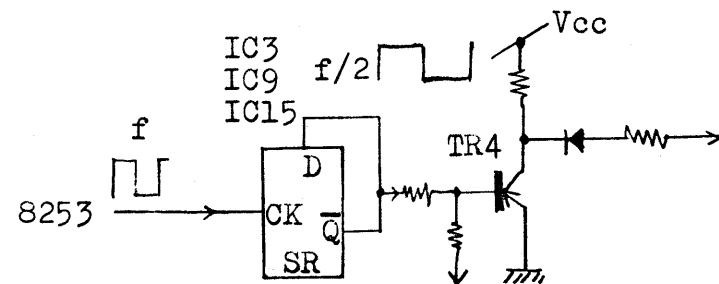


Fig. 4

VCF CONTROL VOLTAGES

While each of 6 contour voltages developed at ENV generator is running to mated VCA on the exclusive line, they are multiplexed and carried through a common bus together with other control signals for VCF application. On the input pin of summing amp., there is another multiplexed voltage KCV from D/A converter IC51-IC53. To prevent garbling of data, de- and multiplexes are synchronized by a clock.

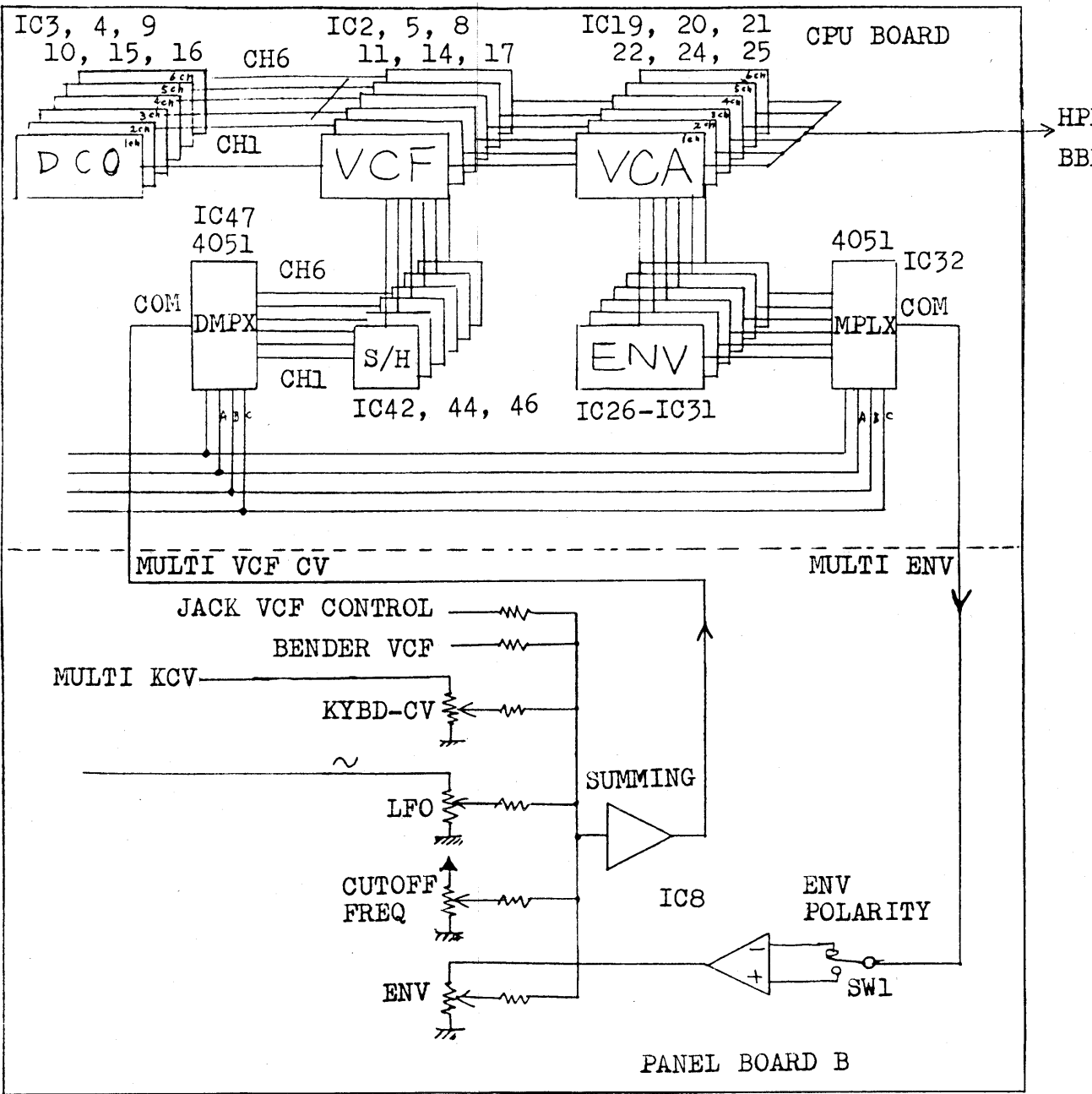
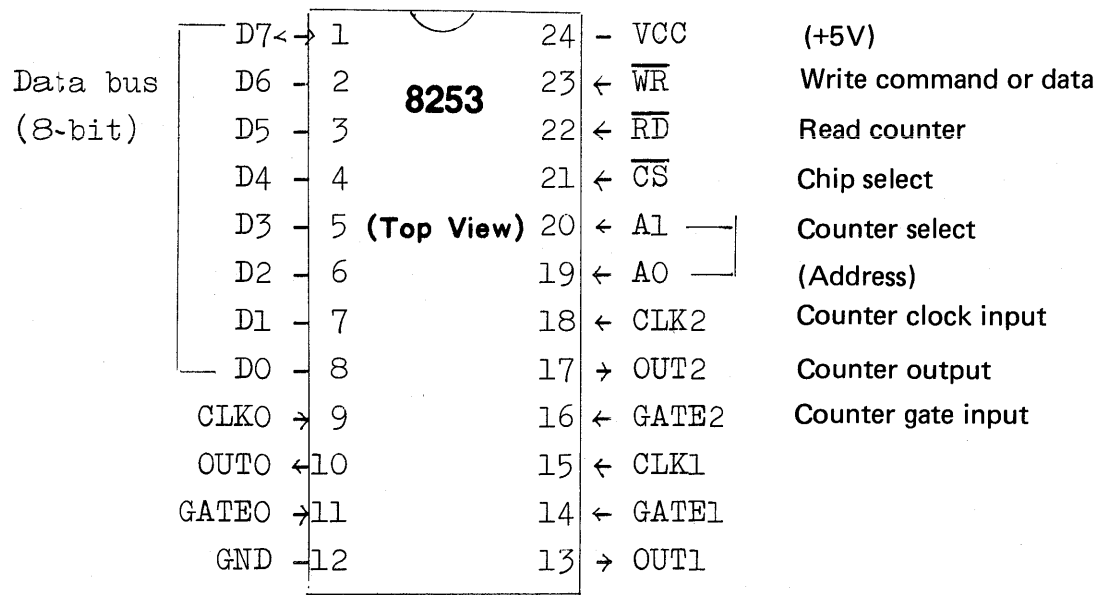


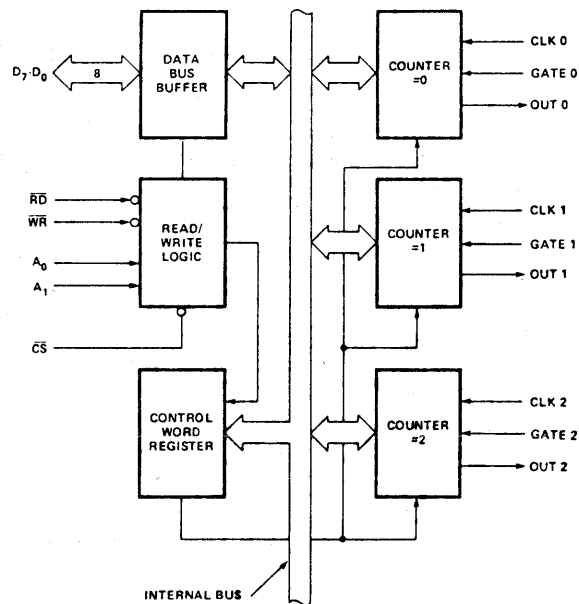
Fig. 5

PROGRAMMABLE INTERVAL TIMER

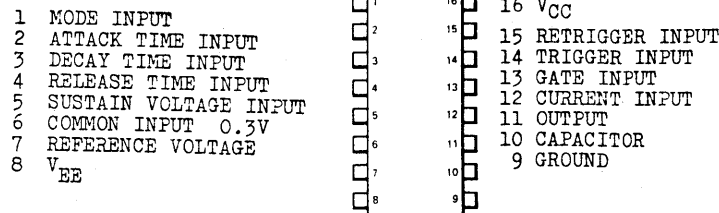


8253

BLOCK DIAGRAM

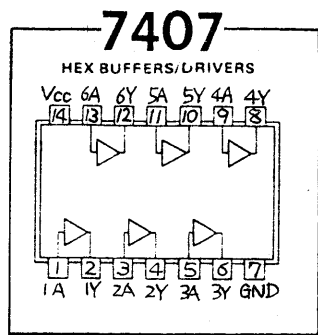
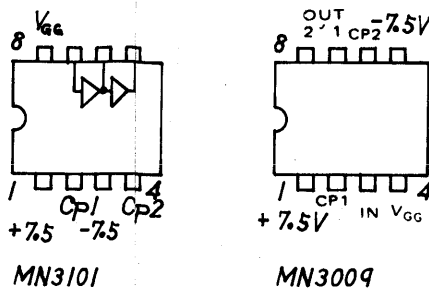


IR3R01



JU-6

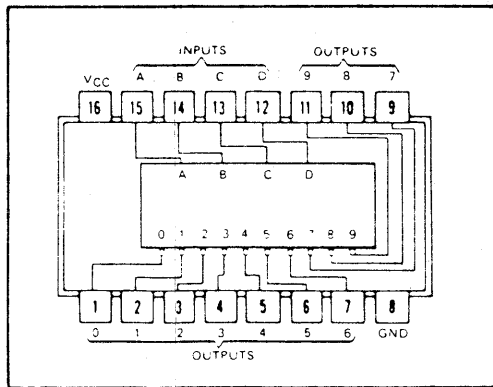
(Top View)



74LS42

ONE-OF-TEN DECODER

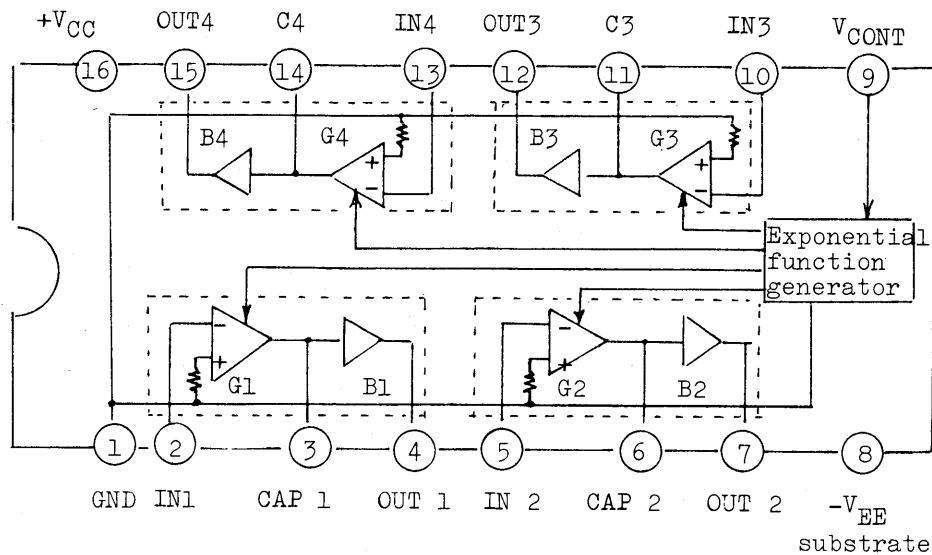
(TOP VIEW)



NO.	'42A, 'L42, 'LS42 BCD INPUT				ALL TYPES DECIMAL OUTPUT									
	D	C	B	A	0	1	2	3	4	5	6	7	8	9
	0	L	L	L	L	L	H	H	H	H	H	H	H	H
1	L	L	L	H	H	L	H	H	H	H	H	H	H	H
2	L	L	H	L	H	H	L	H	H	H	H	H	H	H
3	L	L	H	H	H	H	H	L	H	H	H	H	H	H
4	L	H	L	L	H	H	H	H	L	H	H	H	H	H
5	L	H	L	H	H	H	H	H	H	L	H	H	H	H
6	L	H	H	L	H	H	H	H	H	H	L	H	H	H
7	L	H	H	H	H	H	H	H	H	H	H	L	H	H
8	H	L	L	L	H	H	H	H	H	H	H	H	L	H
9	H	L	L	H	H	H	H	H	H	H	H	H	H	L
INVALID	H	L	H	L	H	H	H	H	H	H	H	H	H	H
	H	L	H	H	H	H	H	H	H	H	H	H	H	H
	H	H	L	L	H	H	H	H	H	H	H	H	H	H
	H	H	L	H	H	H	H	H	H	H	H	H	H	H

IR3109

(top view),

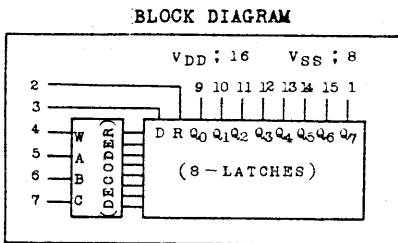


The IR3109 contains four variable transconductance amplifiers designed for VCF applications in electronic musical instruments. The device is equipped with four high input impedance buffers, and anti-log circuitry (V-in to I-out) which controls conductances of four amps.

- wide transconductance variable range (1 μ S–10mS)
- low input offset voltage (less than $\pm$ 3mV) (transconductance amplifier)
- high input impedance, MOS P-channel (buffer)

TC4099BP

8-Bit Addressable Latch



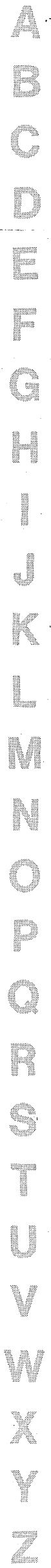
CONTROL INPUTS		ADDRESS INPUTS			OUTPUTS							
RESET	W.DIS.	C	B	A	Q0	Q1	Q2	Q3	Q4	Q5	Q6	Q7
H	H	*	*	*	L	L	L	L	L	L	L	L
L	H	*	*	*	-	-	-	-	-	-	-	-
H	L	L	L	L	D	L	L	L	L	L	L	L
H	L	L	L	H	L	D	L	L	L	L	L	L
H	L	L	H	L	L	L	D	L	L	L	L	L
H	L	L	H	H	L	L	L	D	L	L	L	L
H	L	H	L	L	L	L	L	D	L	L	L	L
H	L	H	L	H	L	L	L	L	L	D	L	L
H	L	H	H	H	L	L	L	L	L	L	L	D
L	L	L	L	L	D	-	-	-	-	-	-	-
L	L	L	L	H	-	D	-	-	-	-	-	-
L	L	L	H	L	-	-	D	-	-	-	-	-
L	L	L	H	H	-	-	-	D	-	-	-	-
L	L	H	L	L	-	-	-	-	D	-	-	-
L	L	H	L	H	-	-	-	-	-	D	-	-
L	L	H	H	L	-	-	-	-	-	-	D	-
L	L	H	H	H	-	-	-	-	-	-	-	D

* : DON'T CARE

D : DATA INPUT

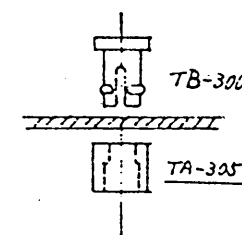
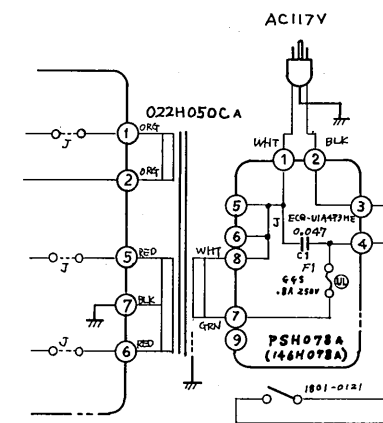
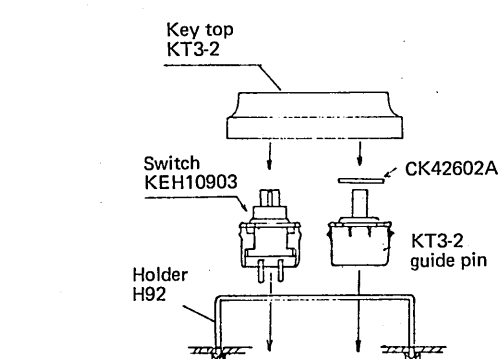
- : HOLDS PREVIOUS DATA

1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20 21 22 23 24 25 26 27 28 29 30 31 32 33 34 35 36 37 38 39 40 41 42 43 44 45

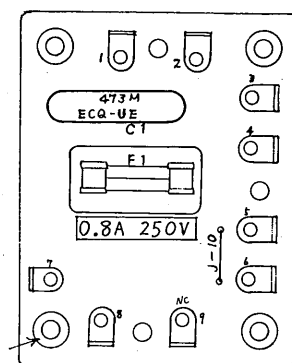


SLE623-18P

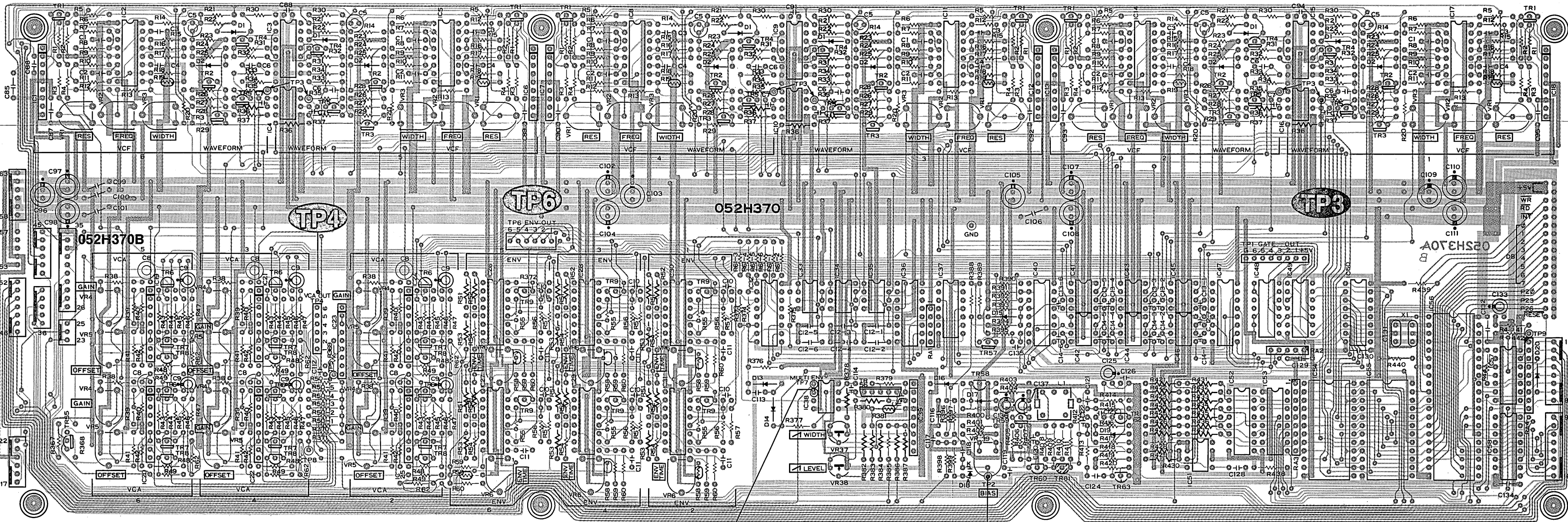
CONCLUSIONS



PT secondary ratings
18V x2 at 0.35A
9.5V x1 at 0.35A



PT secondary ratings
18V x2 at 0.35A
9.5V x1 at 0.35A



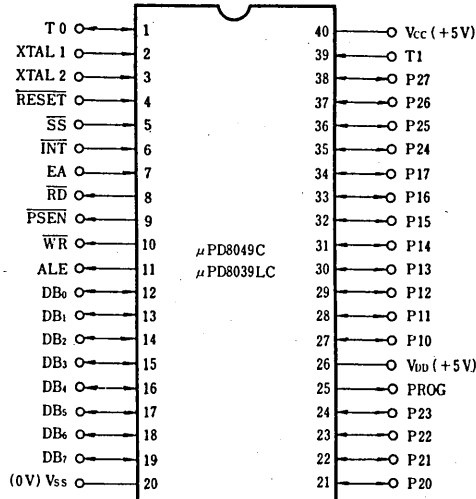
TP7 VR38 VR37 VR39 TP2

μPD8049C-238

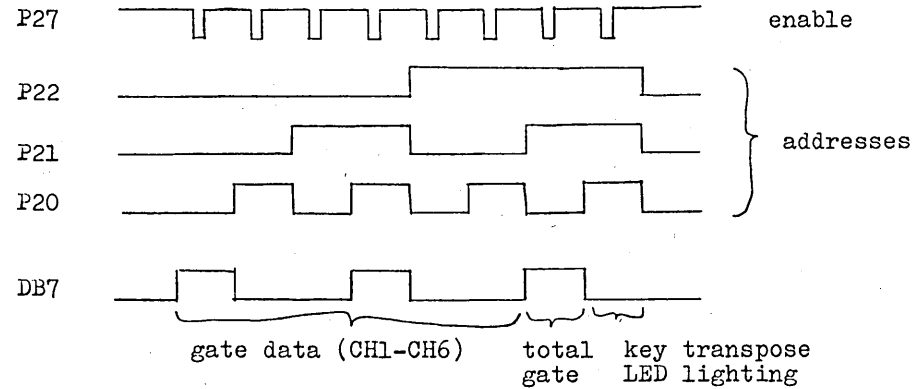
CHANGES IN COMPONENTS

Initial SN	Part	From	To	Reason
150600	IC40, IC47	TC4051BP	HD14051B (only)	increase circuit stability
16800	R372 (IC3R01)	10K	2.7K	increase pin 15 voltage from 5V to 10V
	R389 (TR57)	47K	33K	decrease IC40, IC47 VEE from -12V to -11V
181650	Circuit board	052H370A	052H370B	R62 680K x 4 bottom to top
	R421-R426, R430	49.5K	75K	increase D/A accuracy 0.48V/oct
	R431-R437, R429 R427 (IC52, IC53)	100K	150K	
	R396 (IC58)	1M	680K	balance Bender control voltage
	R397	33K	22K	

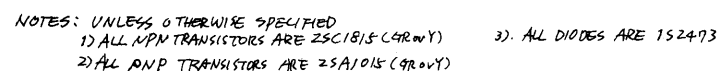
(Top View)



NOTES:
TOTAL GATE ORed 6 gates, issued whenever key(s) has been played after the preceding TOTAL GATE.
INT Must be kept pulled up during operation, otherwise no sound will be generated.

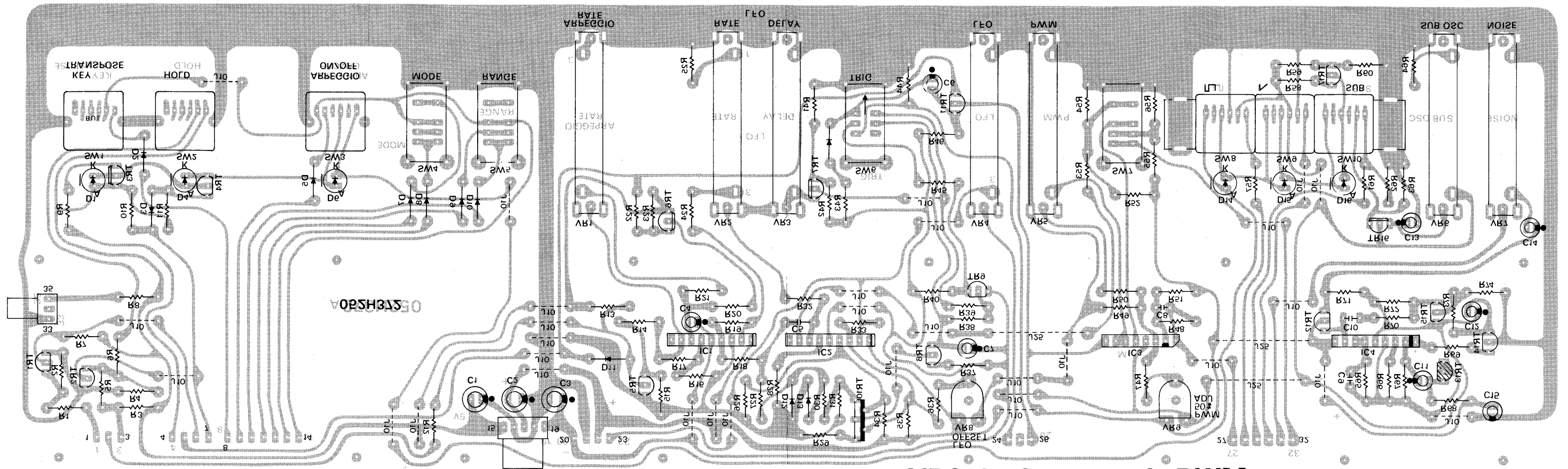


DESIGNATION	PIN NO.	FUNCTION
DB DB 0 (DATA BUS)	12 13 14 15 16 17 18 19	8253 (IC54, 55) Division data KCV data (in synchronous with KCV and GATE addresses)
PORT 1 P10	27 28 29 30 31 32 33 34	keyboard and function switches scanning data read
PORT 2 P20	21 22 23 24 25 26 27	8253 (IC54, 55) address 4099 (IC50) 4051 (IC32, 36, 40, 47) addresses
T0 T1 WR	39 38 10	ARPEGGIO clock input (ON:L OFF:H) 8253 write pulse



1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20 21 22 23 24 25 26 27 28 29 30 31 32 33 34 35 36 37 38 39 40 41

A
B
C
D
E
F
G
H
I
J
K
L
M
N
O
P
Q
R
S
T
U
V

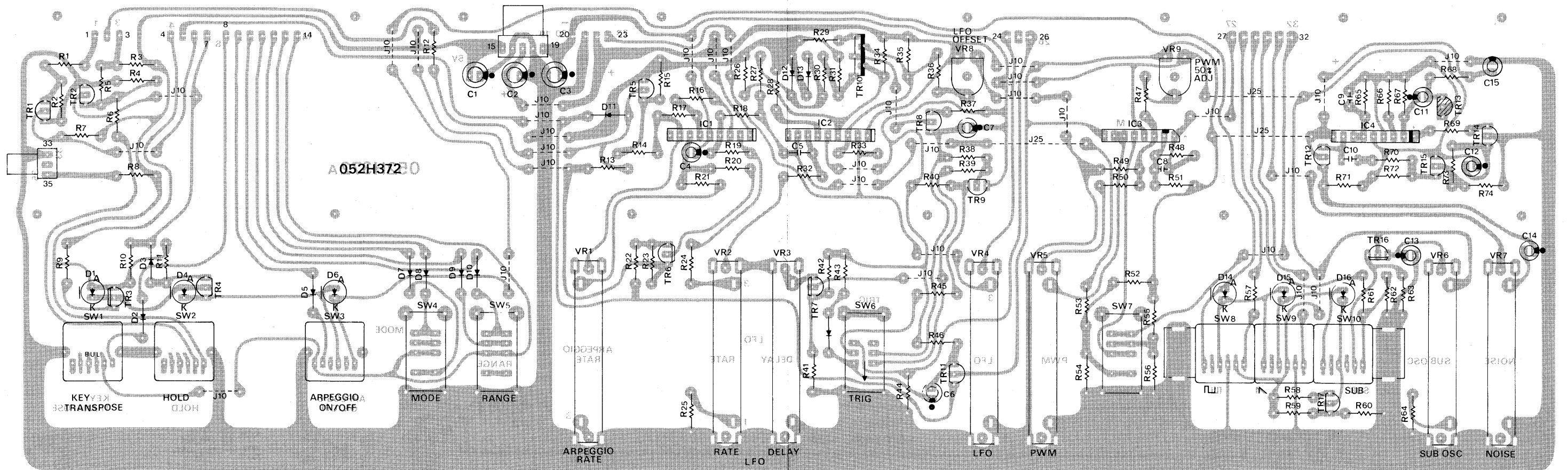


PANEL BOARD A OPH164A(149H164A)(pcb 052H372A)

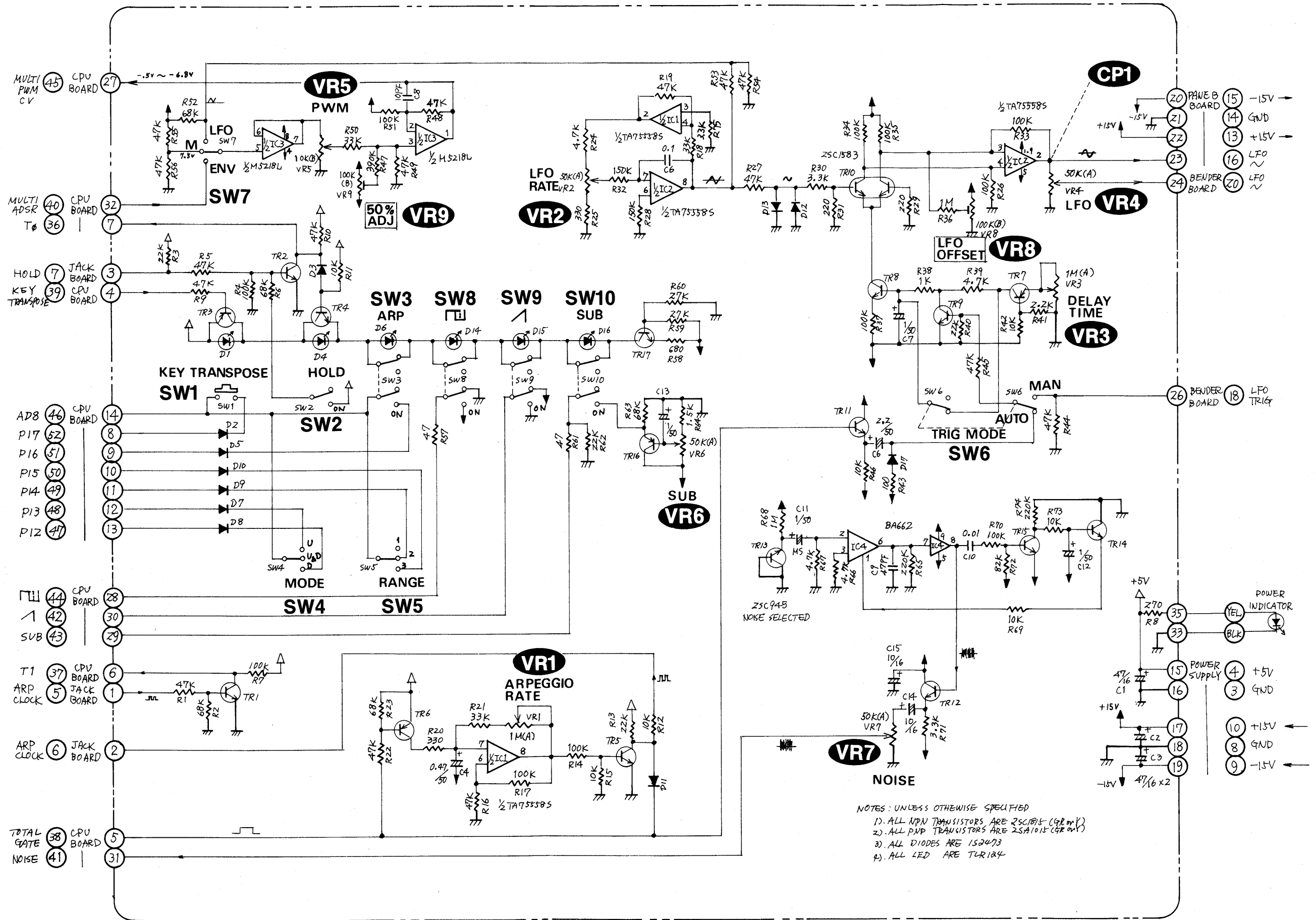
VR8 LFO

VR9 PWM

above bottom view
below top view



- SW1:
SUT11A-1
SW2, 3:
SUT11A-2
(push-lock)
SW4, 5, 7:
SLE623-18P
SW6:
SLE622-18P
SW8-10:
SUT32A-1
(gang)
Button:
white H36
orange H29
yellow H30
- VR1, 3:
EVA-TOHC14A16
VR2, 4, 6, 7:
EVA-TOHC14A54
VR5:
EVA-TOHC14B14



PANEL BOARD B
OPH165A (149H165A)
(pcb 052H373A)

View from foil side

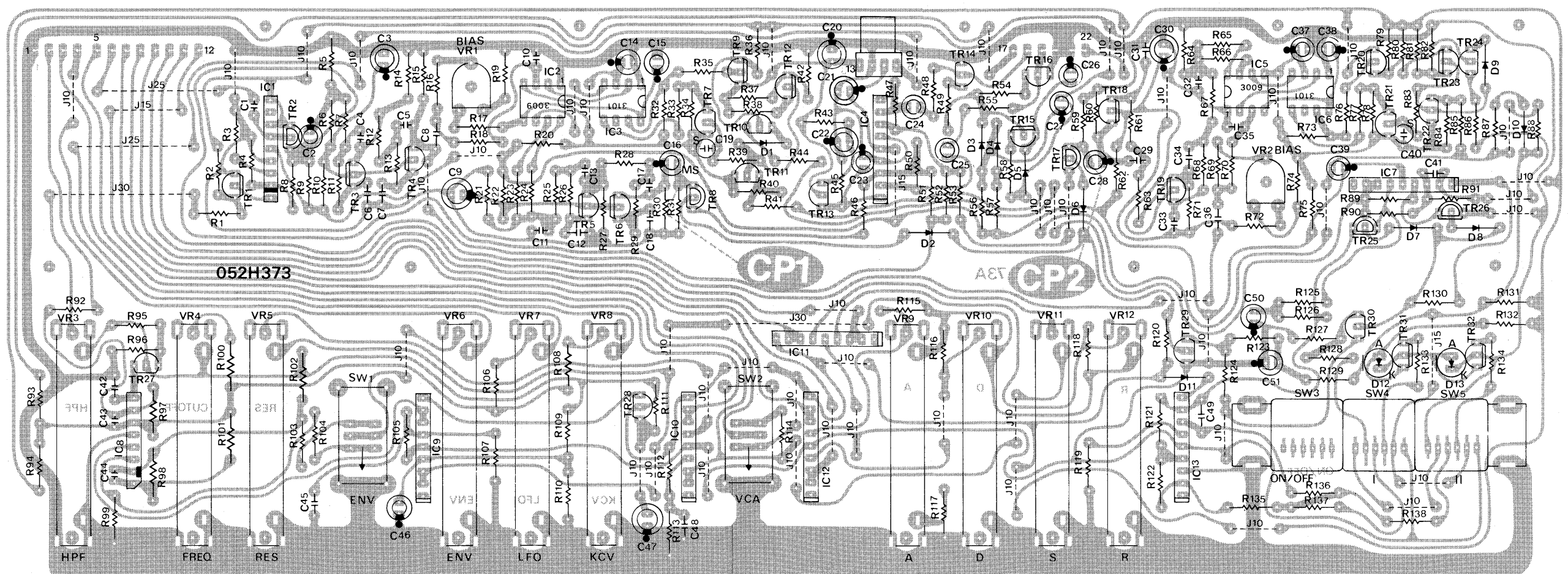
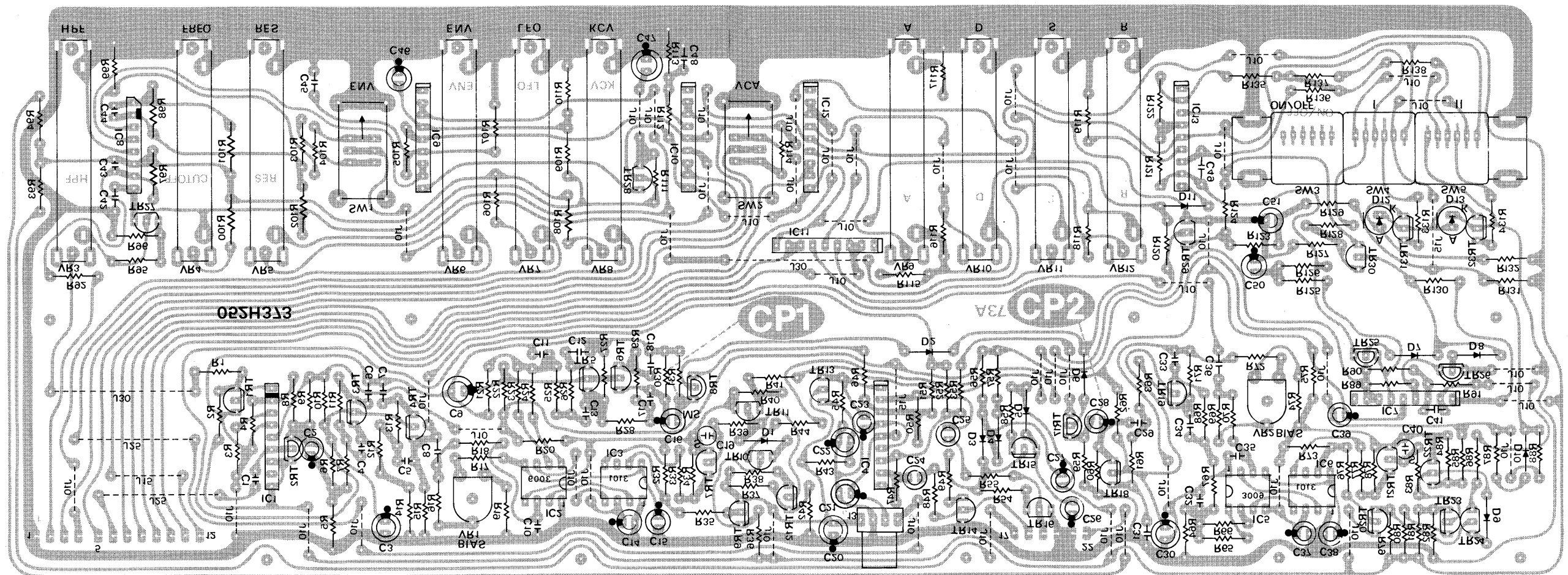
VR3, 4, 5:
EVA-TOHC14B54
VR6, 8:
EVA-TOHC14B14
VR7, 9, 10, 11, 12:
EVA-TOHC14B15

SW1, 2:
SLE622-18P

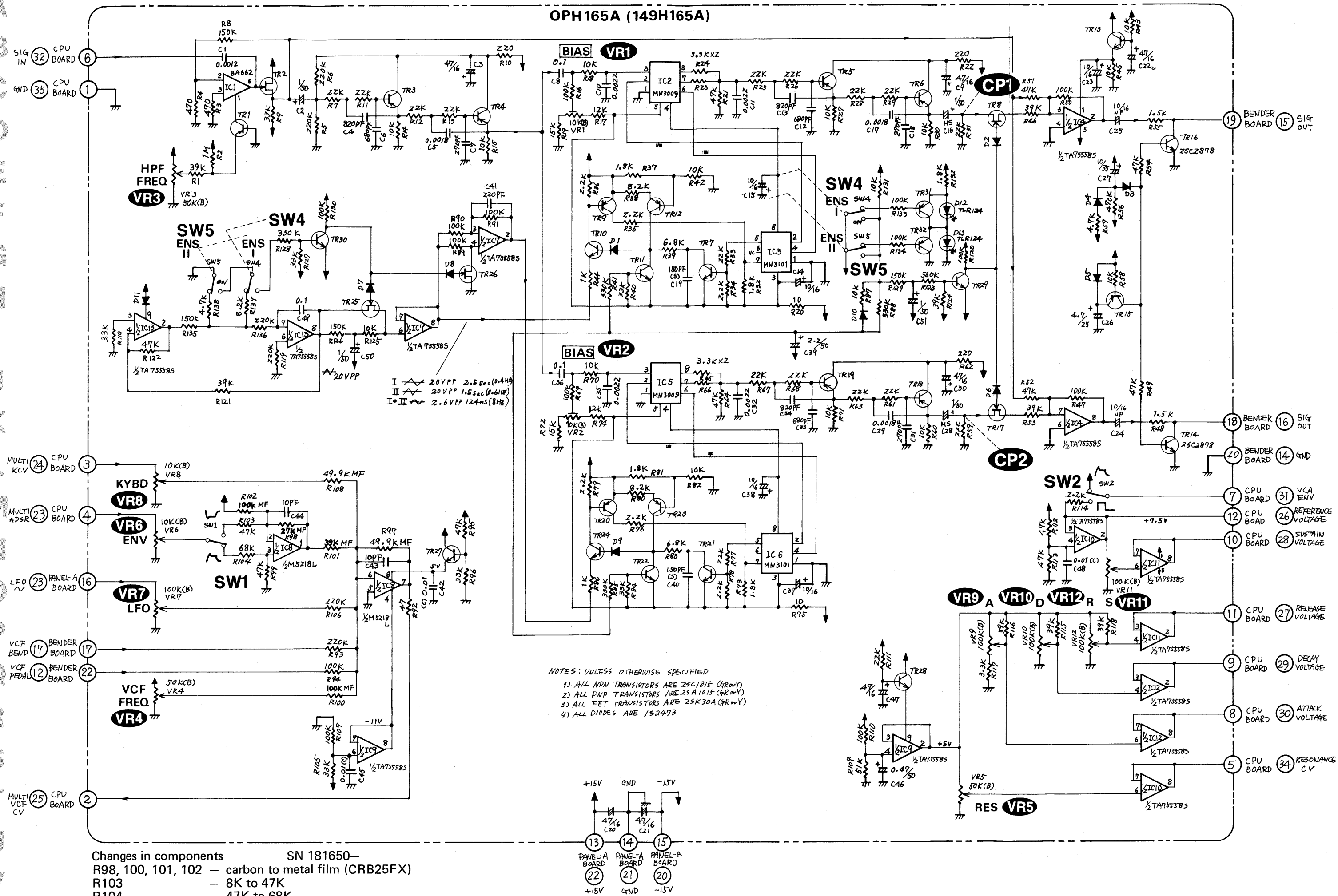
SW3, 4, 5:
SUT32A-2

Button:
white H36
yellow H30
orange H29

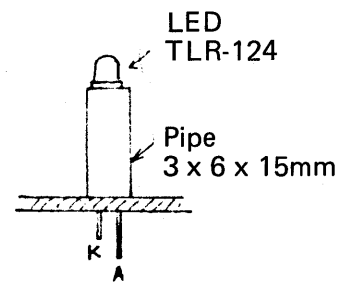
View from
component side



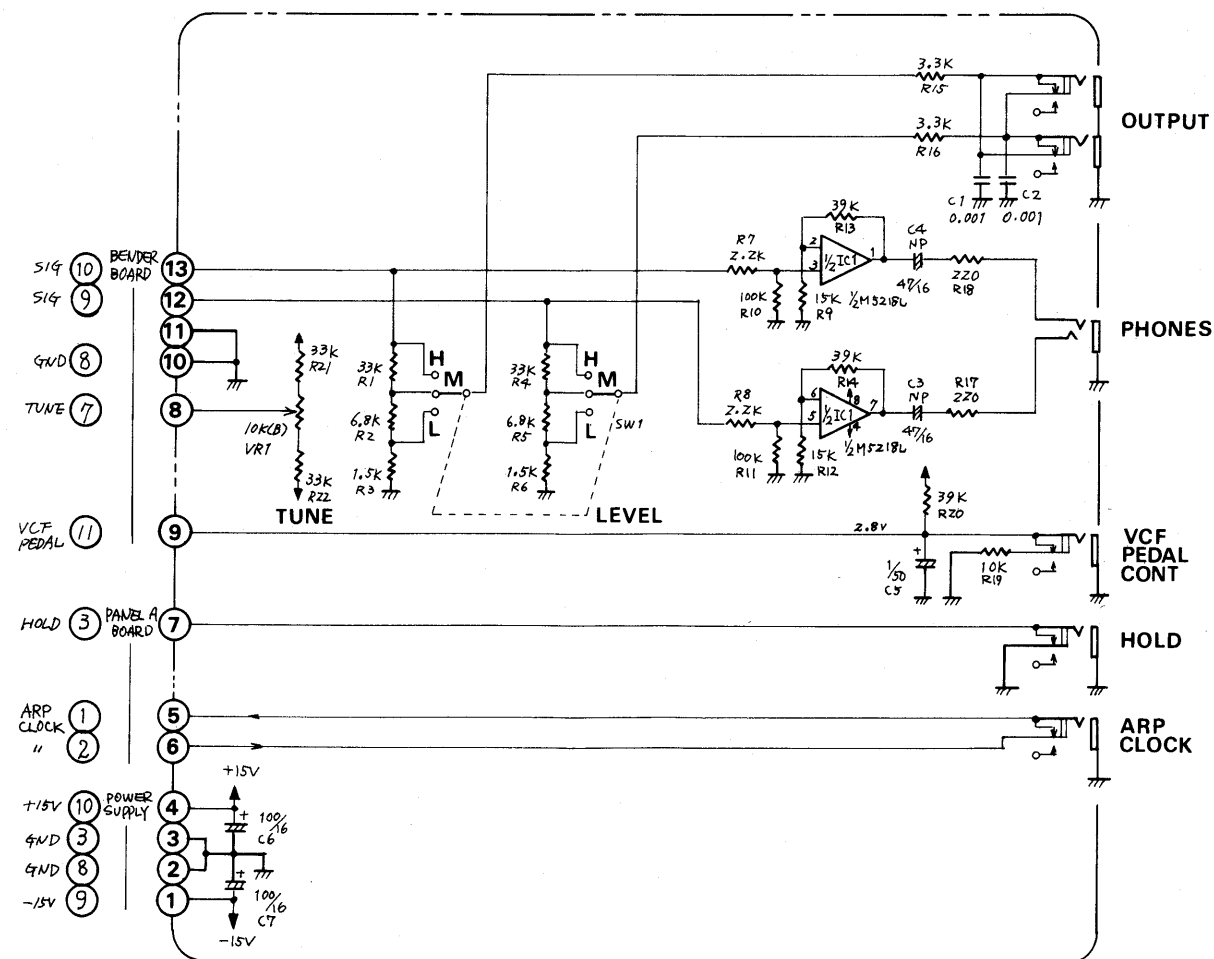
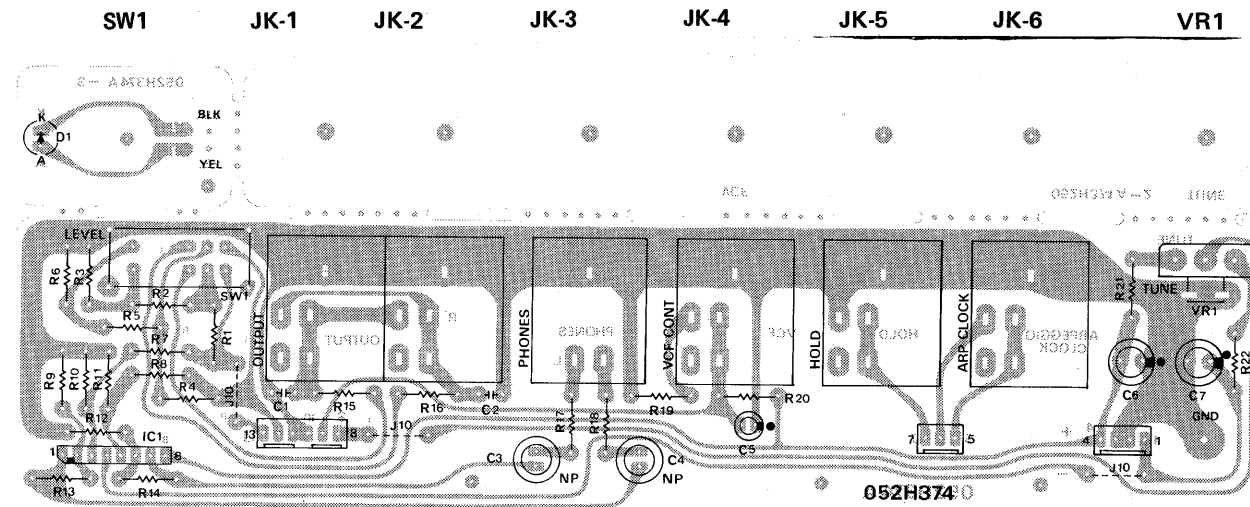
OPH165A (149H165A)



JACK BOARD OPH163A(149H163A)(pcb 052H374A)



SW1	HSW0372-01-030	JK-3	HLJ-0259-01-020
VR1	EVH-OTAS10B14	JK-1, 2, 4, 5, 6	HLJ-0259-01-030



ADJUSTMENT SAMMARY

Use OSCILLOSCOPE unless otherwise specified.
No particular channel, test point, trimmer, etc. are defined in the procedures common to sextuple circuits. Begin with channel 1 (CH1).

KEY ASSIGNMENT

Some adjustments need to be done in unique key assign mode available only in TEST MODE.

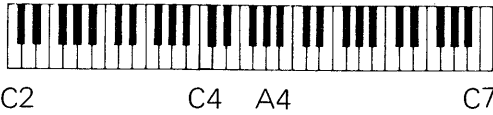
TEST MODE

To enter test mode hold KEY TRANSPOSE until power is ON.
Select key assign mode through ARPEGGIO MODE selector:

- UP (UNISON): six voices sounds simaltenously
- UP & DOWN (ROTARY): as the name implies, CPU assigns channels (in the order numbered, example, 1, 2, ... 6, 1) to the keys played (legato or staccato), and remembers the last channel even after the key is released.
New assignment will start with the next channel. Note that the first key does not always activate CH1.
The above applies to repeated striking on the same key.
- DOWN (NON-ROTARY): The key first played is always assigned CH1. Until the objective channel is assigned, the preceding key(s) can not be released.

To escape TEST MODE turn power OFF. Allow 3 sec for CPU reset circuit before turning on again.

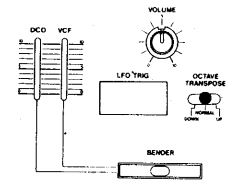
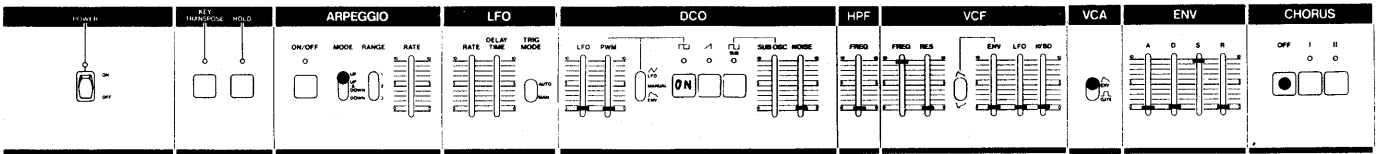
KEY DESIGNATION



DC SUPPLY VOLTAGE (Power Supply Board)

- TEST POINTS: terminal 10 (+15V); terminal 8 (ground) (Connect to digital voltmeter, DVM.)
1. Adjust VR1 for +15±0.01V.
2. Verify voltage of -14.5 to -15.5V at terminal 9 (-15V).

MASTER OSCILLATOR (CPU Board)



- TEST MODE: UP (UNISON)
- CONTROLS: TUNE (rear panel) at midpoint

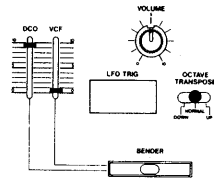
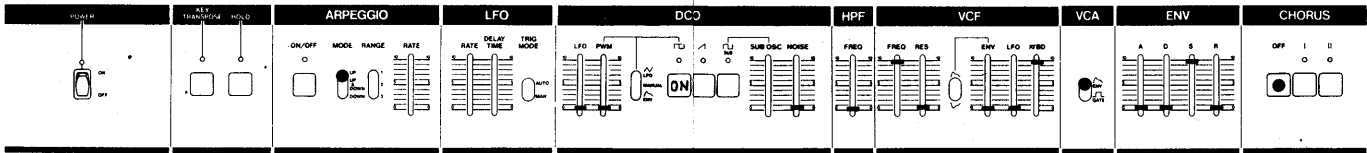
BIAS

- TEST POINT: TP-2 (VR39 wiper) (Connect to scope or DVM. Do not use low impedance meter.)
1. Adjust VR39 for 7.2±0.1V.

TUNING

- TEST POINT: TP-3, pin 10 of IC55 or OUTPUT jack
1. While holding down A4 key, adjust L1 for 442Hz. L1 is very tricky, so readjust VR39 for fine tune, as necessary. This has little effect on BIAS adjustment.

BENDER CONTROL (BENDER Board)



- TEST MODE: UP
- TEST POINT: same as for TUNING, above

1. Use HOLD function. With E5 note on, tilt and hold BENDER lever at the leftmost position and adjust VR1 so that the frequency is 442Hz (A4 note).
2. HOLD D4 key. With BENDER at the rightmost, adjust VR2 so that frequency is 442Hz.

SAWTHOOTH WIDTH & LEVEL (CPU Board)

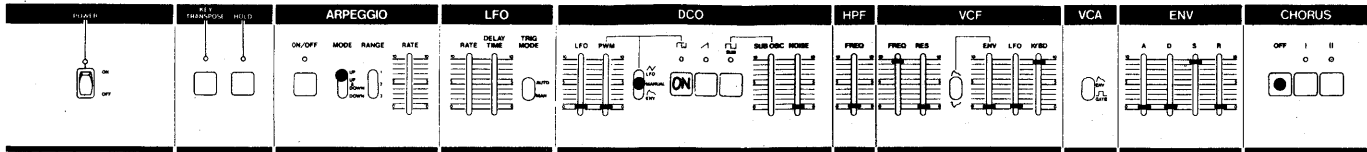
- CONTROLS: OCTAVE TRANSPOSE at NORMAL
- TEST POINT: TP-3
- TEST MODE: UP
1. Set VR37 and VR38 at midpoint.
2. Striking C2 and C7 keys alternately (with break between notes), adjust WIDTH VR37 for the same amplitude on both keys.
3. While holding C4 key down, adjust LEVEL VR38 for 12Vp-p. Next, check TP-3 of the remaining channels (2-6) for 12±0.5Vp-p.

PULSE WIDTH (CPU Board, PANEL BOARD A)

- CONTROLS: DCO section — WAVEFORM-PWM; MODE-MANUAL; PWM slider-0
- TEST POINT: pin 1 (CH1) of TP-4 (CPU board) (scope — 1V/div, 0.2ms/div)
- TEST MODE: UP
1. While holding down B4 key, adjust VR9 of PANEL BRD A for a 496Hz rectangular of duty cycle 50. Check all other channels (pins 2-6) for 48-52 duty cycle.
2. Set PWM slider to 10 and check every pin of TP-4 for 95 to 98% duty cycle.

VCA (CPU Board)

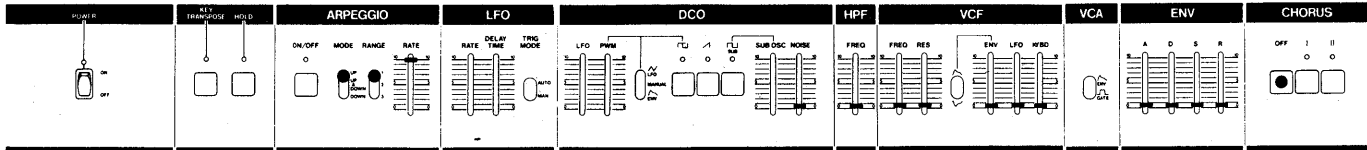
GAIN



- TEST POINT: TP-4 (pins 1-6)
- TEST MODE: UP

1. Depressing C5 key, adjust VCA GAIN VR4 for 4Vp-p.

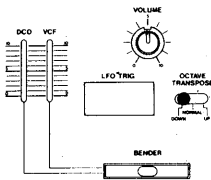
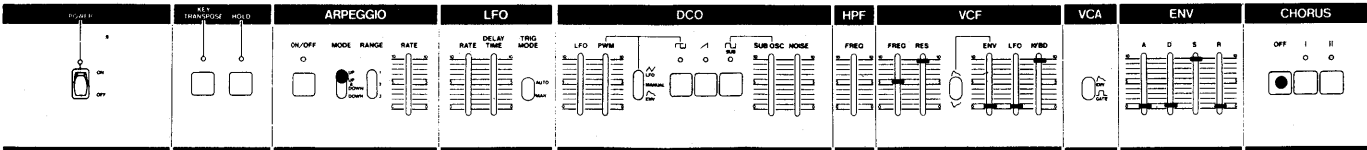
OFFSET



- TEST POINT: TP-4 (pins 1-6) (scope 0.2V/div)
- TEST MODE: Normal (Push ARPEGGIO. This overrides Test Key Assign Mode until pushed again.)

1. HOLD ON more than one note, 6 channels will be gated in sequence.
2. Adjust OFFSET VR5 for reasonable straightness.

VCF (CPU Board)



- TEST POINT: TP-4 (pins 1-6)
- TEST MODE: UP

RESONANCE

1. While pressing C4 key, adjust RES VR1 for 4Vp-p regenerating sine wave.

FREQUENCY

1. With C2 key holding down, set VREQ VR2 at the position where the period of the wave is 4.03ms (248Hz, equal to normal B3 note). (Note, KBD control voltage is 0.)

WIDTH

1. While holding C4 key, adjust WIDTH VR3 for 992Hz.

ENVELOPE (CPU Board)

- CONTROLS: ENV — A at 10; D, S and R at 0
- TEST MODE: UP
- TEST POINT: TP-6 (pin 1) (scope 2V/div 0.5s/div)

1. Set ENV TIME VR6 for 3 sec attack time from a key pressing (CH1 only).
2. Shift scope probe to TP-7 or terminal 23. Reset scope timebase to 50μs/div.
3. Holding down any key will display six growing waves on the scope; CH1 being at the extreme left. Align the rise time of the remaining waves to CH1's (coincidental max. to 0 transitions is desired).
4. Check 6 sounds for synchronization in A, D, S and R phases by sweeping respective sliders.

BBD BIAS (CPU Board.PANEL BOARD B)

- CONTROLS: CHORUS 1
 - TEST POINT: CP1 (R31) — PANEL Board B
1. Feed 5Vp-p, 1kHz, sine wave across TP-8 and ground terminal of CPU board.
2. Set BIAS VR1 for distortion-free waveform.
3. Shift scope to CP2 (R59). Adjust BIAS VR2 as in step 2.

LFO OFFSET (PANEL BOARD A)

- PANEL CONTROLS: LFO TRIG MODE at MAN (CAUTION: Do not touch LEF TRIG.)
 - TEST POINT: CP1 (R33) or terminal 23 (scope DC couple)
1. Adjust OFFSET VR8 for 0±10mV.